Sub-microwatt Correlation Integral Processor for Implantable Closed-loop Epileptic Neuromodulator

Yu-Hsin Chen, Tung-Chien Chen, Tsung-Hsueh Lee, and Liang-Gee Chen
Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, Email: lgchen@cc.ee.ntu.edu.tw

***Abstract*—Neuromodulation of the brain is an emerging therapy to control the epileptic seizure. The therapy can be improved with a closed-loop mechanism in which the electrical stimuli is activated in accordance with the seizure onset. In this paper, a correlation integral (CI) processor in a form of application specific integrated circuit is designed to estimate the brain complexity, chaoticity, after the EEG/ECoG sensors. Since the neural firing becomes more organized prior to the seizure, the intent is to drive the neuromodulator after the early detection of the seizure onset. With the simplified CI algorithm and channel-folded architecture, 0.14μW/channel power consumption is achieved in 90nm CMOS process to simultaneously extract chaoticity for 16 channels in a real time. The simulation results demonstrate a 98.23% and 97.81% of sensitivity and specificity for the classification of normal and epileptic brain rhythms.**

I. Introduction

Neuromodulation of the brain is an emerging therapy to control the epileptic seizure in the last decade. This treatment uses the electrical current pulses to break down the synchronized firing of the epileptic neurons, and has been proven to be effective in some clinical trials [1], [2]. Most of the neuromodulation systems are operated with an open-loop mechanism. In this mechanism the device keeps injecting the current pulses according to the pre-programmed parameters without considering the dynamics of the brain. Recent studies suggest that the percentage of the epileptic patients to be rendered as seizure-free cases could be improved from 0% to 17% [3] if the brain stimulation can be deliberately executed before the seizure onset. Therefore the closed-loop neuromodulator that electrically stimulates the brain according to the brain dynamics is required.

Electroencephalogram (EEG) and electrocorticogram (ECoG) are the physiological signals reflecting the brain dynamics. Unsupervised algorithms have been proposed to extract the features from EEG/ECoG signals and then detect or predict the seizure onset based on the extracted features [4], [5]. Among these algorithms, correlation integral (CI) and correlation dimension (CD) can be used to estimate the chaoticity for the non-linear system of the brain [4], [6]–[8]. Prior to a seizure, neural firing patterns become more organized, causing the decrease of the brain chaoticity, and the CI/CD value becomes one of the important bio-markers for the seizure prediction [9]–[12].

The closed-loop neuromodulation system to control the epileptic seizure is composed of EEG/ECoG sensors, signal processing units, and neuromodulators. The processing units along with the sensor are used to monitor the brain dynamic and activate the prompt feedback control to the neuromodulators once an epileptic seizure is predicted. As the current trend to make the system implantable, the hardware on a miniaturized and low-power VLSI on-chip system is preferred because of the space and power constrains imposed by the applications. Since the brain sensing circuitries in microwatt power consumption have been reported [13], the hardware realization of the seizure early detection algorithms on a similar or lower power level are highly desired. Compared to the general-purpose microprocessor, application specific integrated circuit (ASIC) is more practical for the minimized computational overhead and optimized power dissipation [3], [14]. ISCAS2007-InVitroEpilepticVLSI In this paper, a CI processor in a form of ASIC is designed to extract the brain chaoticity features simultaneously for 16 channels in the closed-loop epileptic neuromodulator. Sub-microwatt power consumption is achieved for the processor after the computational complexity reduction through the algorithm modification and the leakage power saving through the hardware sharing among channels. The paper is organized as follows. We introduce the proposed closed-loop neuromodulation system in Section II and review the CI algorithm in Section III. In Section IV, the hardware architecture is proposed with several low-power design considerations. The simulation and implementation results are described in Section V. Finally the conclusion is made in Section VI.

II. The Closed-loop Neuromodulation System

The closed-loop neuromodulation system for epilepsy control is an implantable miniaturized device featuring neurostimulator and neuro-signal processing units. Such power-limited application demands ultra low-power implementation from every design consideration. For example, computational complexity and hardware area should be maintained at a minimum to decrease dynamical power and leakage power consumption, respectively. Also, ASIC realization with more advanced process could benefit the power dissipation performance.

A. System Architecture

Fig. 1 shows the detailed block diagram of the proposed closed-loop neuromodulation system, which simultaneously processes M channels of EEG/ECoG. The system features three sequential operation stages: 1) the front-end analog circuit for EEG/ECoG recording, 2) the digital signal processing unit (DSPU) and 3) the multi-channel neurostimulator. The M-channel EEG/ECoG sensed by the electrodes are amplified, digitized and time-multiplexed by the front-end circuit. Then, the DSPU processes M-channel signals for early identifying of upcoming seizures. When seizures are detected, the N-channel

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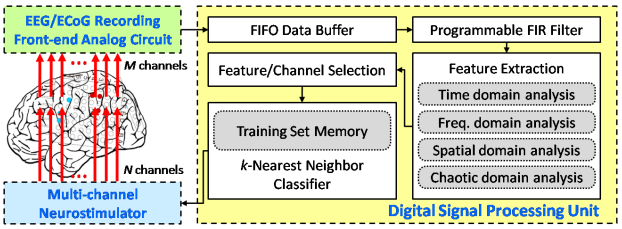


Fig. 1. The block diagram of the closed-loop neuromodulation system.

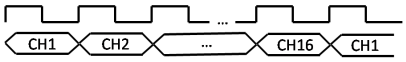


Fig. 2. The 16-channel time-multiplexed EEG/ECoG to the DSPU.

neurostimulator would send stimulating current to break down the epileptic neural firing.

The DSPU mainly comprises the programmable FIR filter for signal preprocessing, the feature extraction module for epileptic EEG/ECoG characterization and the k-nearest neighbor (KNN) classifier for epileptic feature decision. Multi-feature scheme is applied to enhance the detection accuracy from time, frequency, spatial and non-linear chaotic domain analysis. Feature/channel selection is performed to preserve useful information and reduce total data quantity.

B. System Specification

Our design targets at the system with 16 channels processing capability, i.e. M = 16. The sampling rate of EEG/ECoG from each channel is 256Hz with input bit precision of 9 bits, and the system clock rate becomes 4096Hz by multiplexing signals from 16 channels as shown in Fig. 2 for DSPU operation. To achieve real time detection response, the detection interval, which is also the feature update period, is set to be 0.1 second. For linear measures, curve length (CL) [15], rhythmic discharge (RD) [16] and mean phase coherence [17] are adopted for time, frequency and spatial domain analysis. For non-linear chaotic analysis, correlation integral is applied.

III. The Correlation Integral

Correlation integral (CI) and Correlation dimension (CD) are commonly used non-linear features for system chaoticity estimation in epilepsy researches. For its calculation, it should be noted that the complexity of the ECoG signal is reflected in its dimension [18]. Therefore, the ECoG time series should be mapped to a vector-valued phase space in higher dimension for further analyses. Let the ECoG time-domain samples and the embedding dimension of the ECoG signals be denoted by $\{x_i\}$ and p, respectively. The vector V_i in the phase space could be constructed using time-delay coordinates [18] as

$$V_i = (x_i, x_{i+\tau}, x_{i+2\tau}, \ldots, x_{i+(p-1)\tau}), \tag{1}$$

where τ is the selected delay time between the components of each vector in the phase space. For ECoG, p could be set to 7 and τ should be about 14 msec [18].

The correlation integral is defined as [6]

$$C(\varepsilon) = \frac{2}{N(N-1)} \sum_{i=1}^{N} \sum_{j=1, j\neq i}^{N} \Theta(\varepsilon - \|V_i - V_j\|), \tag{2}$$

where N is the number of vectors under consideration, ε is the distance threshold, $\|.\|$ calculates the distance between the vectors, and $\Theta(.)$ is the Heaviside step function. From the definition of CI, the correlation dimension is then given by [6]

$$D_2 \approx \lim_{\varepsilon\to\infty} \lim_{N\to\infty} \frac{\log C(\varepsilon)}{\log \varepsilon}. \tag{3}$$

The above formula indicates that CD is estimated based on CI. Besides, if taken as a measure itself, CI has the advantages of better sensitivity, lower computational complexity and higher noise tolerance when compared to CD [8].

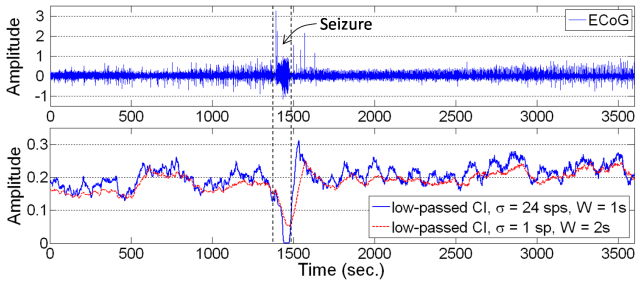


Fig. 3. The ECoG waveform and the corresponding low-passed CI values under different parameter sets. The seizure happens at 1358 to 1475 second.

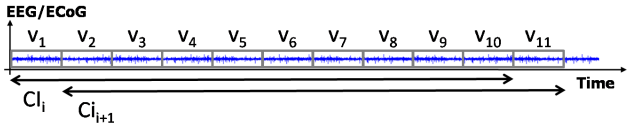


Fig. 4. The phase vector groups, V_1 through V_{10} and V_2 through V_{11}, for consecutive CI computation, CI_i and CI_{i+1}, overlap with each other by 9 vectors, V_2 through V_{10}, which enables the differential scheduling scheme for computational complexity reduction.

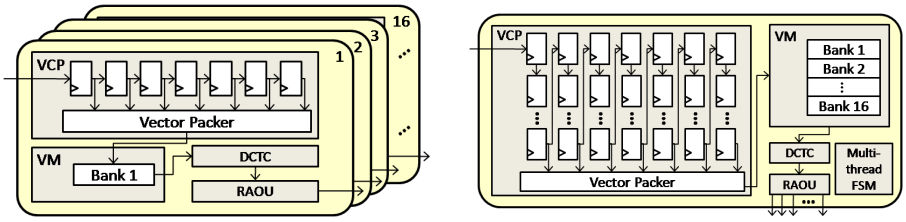
IV. Hardware Architecture Design

As shown in section III, the CI computation consists of three processing stages: 1) the phase space vector collecting and packing from EEG/ECoG (VCP), 2) the vector-pair distance computation and threshold comparison (DCTC) and 3) the comparison result accumulation and output update (RAOU). A vector memory (VM) is required to store vectors from VCP for DCTC and RAOU processing. To realize the multi-channel CI processor with low power consumption, the computational complexity and the hardware area are two design challenges.

A. Reduction on Computational Complexity and Memory Size

The definition of CI in eq. (2) implies that the computational complexity as well as the dynamical power consumption is directly proportional to N^2. The size of VM, which affects the leakage power, is also proportional to N. Therefore, the determination of N becomes a critical issue.

N is decided by two factors: 1) the vector sampling period σ and 2) the window time W. σ indicates the collecting interval of consecutive vectors from EEG/ECoG. If the first component of vector V_i is x_i, the first component of V_{i+1} would be $x_{i+\sigma}$. W is the total vector acquisition time for one CI computation. To decrease N, larger σ with smaller W is preferred. However, large σ might sacrifice the chaotic-dynamics discriminating performance. On the other hand, short window time could result in inaccurate chaoticity estimation but increase the CI sensitivity to abrupt EEG/ECoG changes and shorten the CI computation latency [8].



(a) Single-channel CI processors (b) Multi-channel CI processor

Fig. 5. Multi-channel CI processor is achieved by channel folding and multi-thread hardware sharing from the single-channel one.

TABLE I
SYNTHESIS RESULTS OF CI GENERATOR IN DIFFERENT PROCESSES

CMOS Process	Core Area (μm^2)	Dynamic Power (nW)	Leakage Power (μW)
90nm LL	107189	73.92	2.27
0.13μm	187948	166.18	104.52

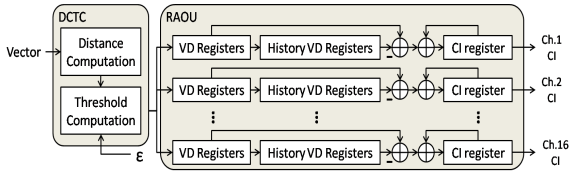


Fig. 6. The DCTC and RAOU module for the multi-channel CI processor.

For conventional application of CI for seizure study, W = 2s and σ = 1 sample have been adopted for analysis [8]. We further decrease W to 1s and increase σ to 24 samples. Note that σ of 24 samples is the sparse-most period for the vectors to cover all EEG/ECoG. Simulations are performed with real long-term ECoG data recorded during presurgical monitoring of 21 patients at the Epilepsy Center of the University Hospital of Freiburg, Germany. Fig. 3 shows the result of ECoG waveform with corresponding low-passed CI values for patient 3 as an example. For both parameter sets, lower CI values could be clearly identified at the seizure stage. The qualitative nature of the curves is unaffected, and the result validates the application of the proposed parameter set for implementation.

The original σ and W have the corresponding N of 488, while the new ones have the N of 10. By the decrease of N, the computational complexity as well as the dynamical power has been substantially lowered by 99.96%. The size of VM is also reduced from the original 492kb to 10kb for total 16 channels, which contributes to the reduction on leakage power.

B. Differential Scheduling for DCTC and RAOU

With N of 10, eq. (2) indicates that total 45 pairs of vector distance (VD) computation, $\Theta(\varepsilon - \|V_i - V_j\|)$, should be performed for one CI value generation per channel. Under the feature update period of 0.1 second and EEG/ECoG sampling rate of 256Hz, Fig. 4 shows that the vector groups, V_1 through V_{10} and V_2 through V_{11}, for consecutive CI computation, CI_i and CI_{i+1}, actually overlap with each other by 9 vectors, V_2 through V_{10}. 9 vectors and total 36 pairs of VD are the same for consecutive CI computation, and only 9 pairs of VD should be recalculated. Therefore, we propose the differential scheduling scheme for more complexity reduction at DCTC and RAOU. Instead of 45 pairs of VD calculation, the update of new CI value at RAOU comes from the old value plus the difference of 9 changed VD pairs, and the DCTC only compute the 9 changed VD pairs for one CI update. With the differential scheduling scheme, the computational complexity is further lowered by 80%, which decreases the dynamical power consumption too.

TABLE II
SIMULATION RESULT OF SEIZURE DETECTION

Feature	Sensitivity (%)	Specificity (%)
CI(original)	99.4286	98.2118
CI(proposed)	98.2286	97.8118

C. Channel Folding with Multi-thread Hardware Sharing

Fig. 5(a) shows the architecture of a single-channel CI processor. VCP contains the FIFO registers for vector collecting and VM has only 1 bank for the storage of 10 vectors. For simultaneous multi-channel processing, parallel implementations of single-channel CI processors shown in Fig. 5(a) would consume large silicon area and result in high leakage power consumption. Thus, the concept of channel folding with multi-thread hardware sharing is proposed. By combining the FIFO registers to form the systolic register array, only one VCP module and one 16-bank VM is required as shown in Fig. 5(b). Folding among channels turns the original 16 10x63bits VM into only one 160x63 bits VM. The area of VM is reduced from $0.135mm^2$ to $0.027mm^2$, and the leakage power consumption corresponding to VM is decreased by 80%. Multi-thread execution is applied for further hardware sharing. Consider the computation of each channel as a thread, a multi-thread FSM is featured to schedule the sharing of DCTC and RAOU for total 16 channels in a time-multiplexed fashion, and 93.75% area is saved for the DCTC and RAOU module implementation.

The architecture of DCTC and RAOU based on the differential scheduling and multi-thread hardware sharing is shown in Fig. 6. 16-channel operations share one DCTC unit, and each channel possesses a corresponding bank in RAOU. The VD registers memorize the 9 changed VD, and a subtraction is applied to compute the difference of the 9 changed VD with that in the history VD registers. The CI register is updated by the accumulation of the old CI value with the 9 changed VD. 16-channel CI computations could be completed within 0.1 seconds simultaneously.

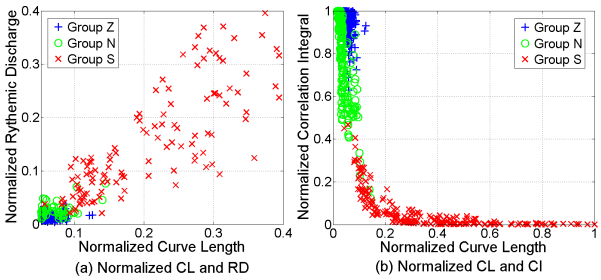


Fig. 7. The feature space distribution of the EEG data with normalized feature (a) CL and RD and (b) CL and CI.

V. Simulation and Implementation Results

A. Simulation Results

The 16-channel CI processor is tested for the ability of seizure detection with a general KNN classifier shown in Fig. 1. The EEG data applied are recorded for normal (group Z), interictal (group N) and epileptic (group S) subjects from the Epilepsy Center at the University of Bonn, Germany. The data are made available online by Dr. R. Andrzejak (http://www.meb.uni-bonn.de/epileptologie/ science/physik/eegdata.html).

Table II shows the detection sensitivity and specificity of the CI feature with original computing algorithm and the proposed algorithm. The simulation results show that the CI with proposed algorithm achieves the detection sensitivity of 98.23% and specificity of 97.81%, which performs as well as the original one. But the implementation cost is greatly reduced as shown in section IV.

Fig. 7 shows the example of EEG data in the feature space with several different features. When only linear features, CL and RD, are used as shown in Fig. 7(a), the boundary of the three groups are not very clear. However, with the aid of the non-linear feature CI shown in Fig. 7(b), the epileptic data(group S) could be easily distinguished from the other two groups, and a transition from the normal data to interictal data, and finally to the ictal data could be discovered.

B. Implementation Results

We use different CMOS processes to implement the proposed CI processor for the given specification. Table I summarizes the synthesis results. Different from ordinary chip designs, the power consumption of the CI processor is dominated by the cell leakage power because of the low clock rate. Thus, we take advantage of the 90nm low-leakage (LL) process to minimize the leakage power. As shown in the table, the leakage power of 90nm LL process implementation is reduced by 97.8% when compared to the 0.13μm implementation. While recently proposed architecture for neuro-signal processing usually consume the power at 10 to 20μw/channel, the proposed CI processor only consumes the power at 0.14μw/channel. Fig. 8 shows the chip layout of the CI generator in 90nm CMOS LL process, and the entire core area becomes $0.143mm^2$.

VI. Conclusion

In this paper, a 16-channel CI processor for epileptic seizure detection is proposed. The detection ability of this design

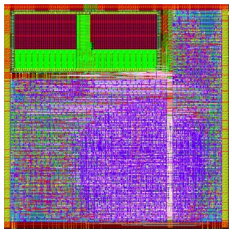


Fig. 8. The layout of the proposed CI generator in 90nm LL CMOS process.

achieves the detection sensitivity of 98.23% and specificity of 97.81%. Also, the synthesis result and layout shows that the CI processor in 90nm LL process has the core area of $0.143mm^2$ and the power consumption of 0.14μW/channel. The CI processor provides an solution for real-time EEG/ECoG processing with low power consumption, which is applicable to the seizure detection part of a closed-loop epileptic neuromodulation system.

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